

## Design of A Efficient Hybrid Adder Using Qca

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**ABSTRACT :** As transistors decrease in size more and more of them can be accommodated in a single die, thus increasing chip computational capabilities. However, transistors cannot get much smaller than their current size. The quantum-dot cellular automata (QCA) approach represents one of the possible solutions in overcoming this physical limit, even though the design of logic modules in QCA is not always straightforward. In this brief, we propose a new adder that outperforms all state - of -the art competitors and achieves the best area - delay tradeoff. The above advantages are obtained by using an overall area similar to the cheaper designs known in literature. The 64 - bit version of the novel adder spans over 18.72  $\mu$  m<sup>2</sup> of active area and shows a delay of only nine clock cycles, that is just 36 clock phases.

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### I. INTRODUCTION

Nanotechnology draws much attention from the public now-a-days. Because the current silicon transistor technology faces challenging problems, such as high power consumption and difficulties in feature size reduction, alternative technologies are sought from researchers. Quantum-dot cellular automata (QCA) is one of the promising future solutions. Since it was first introduced in 1993, experimental devices for semiconductor, molecular, and magnetic approaches have been developed. Quantum dot cellular automata, which is an array of coupled quantum dots to implement boolean logic functions. The advantage of QCA is high packing densities due to the small size of the dots, simplified interconnection and low area delay product.

### II. ADDERS

In electronics, an adder or summer is a digital circuit that performs addition of numbers. In many computers and other kinds of processors, adders are used not only in the arithmetic logic unit(s), but also in other parts of the processor, where they are used to calculate addresses, table indices, and similar operations. Although adders can be constructed for many numerical representations, such as binary-coded, decimal or excess-3, the most common adders operate on binary numbers. In cases where two's complement or ones' complement is being used to represent negative numbers, it is trivial to modify an adder into an adder-subtractor. Other signed number representations require a more complex adder. Adders are fundamental circuits for most digital systems and several adder designs in QCA have been proposed, and a performance comparison was improved. Better adder performance depends on minimizing the carry propagation delay and reducing the area.

### III. QUANTUM DOT CELL

In 1993, Lent et al. proposed a physical implementation of an automaton using quantum dot cells. The automaton quickly gained popularity and it was first fabricated in 1997. Lent combined the discrete nature of both cellular automata and quantum mechanics, to create nano-scale devices capable of performing computation at very high switching speeds and consuming extremely small amounts of electrical power. Today, standard solid state QCA cell design considers the distance between quantum dots to be about 20 nm, and a distance between cells of about 60 nm. Quantum dot Cellular Automata are based on the simple interaction rules between cells placed on a grid. A QCA cell is constructed from four quantum dots arranged in a square pattern. These quantum dots are sites electrons can occupy by tunneling to them. Because of Coulombic repulsion, the two electrons will always reside in opposite corners. The locations of the electrons in the cell (also named polarizations  $P$ ) determine two possible stable states that can be associated to the binary states 1 and 0. Although adjacent cells interact through electrostatic forces and tend to align their polarizations, QCA cells do not have intrinsic data flow directionality. The basic QCA cell consists of four quantum dots in a square array coupled by tunnel barriers. The physical mechanism for interaction between dots is the Coulomb interaction and the quantum-mechanical tunneling. Electrons are able to tunnel between the dots, but they cannot leave the cell. If two mobile electrons are placed in the cell, in the ground state and in the absence of external electrostatic influence, Coulomb repulsion will force the electrons to dots on the opposite corners. The Figure 1 shows a simplified diagram of a quantum-dot cell.

If the cell is charged with two electrons, each free electron to tunnel to any site in the cell, these electrons will try to occupy the furthest possible site with respect to each other due to mutual electrostatic repulsion. Therefore, two distinguishable cell states exist. Figure 2 shows the two possible minimum energy states of a quantum dot cell. The state of a cell is called its polarization, denoted as P. Although arbitrarily chosen, using cell polarization P = -1 to represent logic "0" and P = +1 to represent logic "1" has become standard practice.

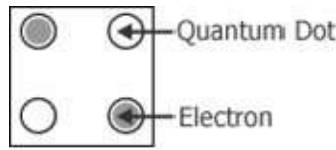


Fig 1: Simplified Diagram of QCA Cell

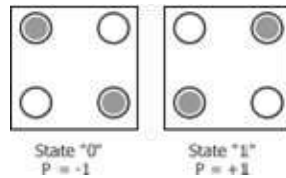


Fig 2: Four Dot Quantum Cell

#### IV. LOGIC GATES

The logic elements of QCA are an inverter and majority gate. An inverter is designed by positioning cells diagonally from each other to achieve the inversion functionality. A majority gate consists of five QCA cells that realize the function of  $M(a; b; c) = ab + bc + ac$ . Two-input AND gate and OR gates can be designed by fixing one of the majority gate inputs to "0" and "1", respectively shown as follows.

$$\text{AND} = M(a,b,0)$$

$$\text{OR} = M(a,b,1)$$

If one input is set to 0, then the output is the AND of the other two inputs. If one input is set to 1, then the output is the OR of the other two inputs. With ANDs, ORs, and inverters, any logic function can be realized.

*Carry-lookahead* is arguably the most important technique in the design of fast adders, especially large ones. In straightforward addition, e.g. in a ripple adder, the operational time is limited by the (worst-case) time allowed for the propagation of carries and is proportional to the number of bits added. So faster adders can be obtained by devising a way to determine carries before they are required to form the sum bits. Carry-lookahead does just this, and, in certain cases the resulting adders have an operational time that is independent of the operands' word-length. A carry,  $C_i$ , is produced at bit-stage  $i$  if either one is *generated* at that stage or if one is *propagated* from the preceding stage. So a carry is generated if both operand bits are 1, and an incoming carry is propagated if one of the operand bits is 1 and the other is 0. Let  $P_i$  and  $G_i$  denote the generation and propagation, respectively, of a carry at stage  $i$ ,  $A_i$  and  $B_i$  denote the two operands bits at that stage, and  $C_{i-1}$  denote the carry into the stage. Then we have

$$G_i = A_i B_i$$

$$P_i = A_i \oplus B_i$$

$$C_i = G_i + P_i C_{i-1}$$

and the sum can be written as  $S_i = P_i \oplus C_{i-1}$  which allows the use of shared logic to produce  $S_i$  and  $P_i$ .

$$C_0 = G_0 + P_0 C_{-1}$$

$$C_1 = G_1 + P_1 P_0 C_{-1} + P_1 G_0$$

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$$C_i = G_i + P_{i-1} G_{i-1} + P_i P_{i-1} G_{i-2} + \dots + P_i P_{i-1} P_{i-2} \dots P_0 C_{-1}$$

where  $C_{i-1}$  is the carry into the adder. The equation for  $C_i$  states that there is a carry from stage  $i$  if there is a carry generated at stage  $i$ , or if there is a carry that is generated at stage  $i-1$  and propagated through stage  $i$  or if, or if the initial carry-in,  $C_{-1}$ , is propagated through stages  $0, 1, \dots, i$ . The complete set, of equations show that, in theory at least, all the carries can be determined independently, in parallel, and in a time (three gate delays) that is independent of the number of bits to be added. The same is also therefore true for all the sum bits, which require only one additional gate delay.

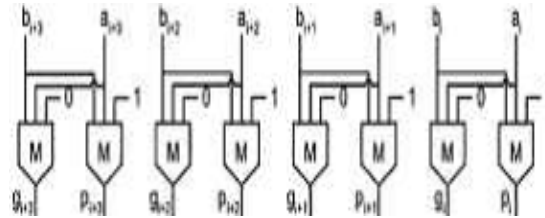


Fig 7: Generation of propagate and generate bits

$G_i = A_i B_i$   
 $P_i = A_i \oplus B_i$

Compared with a ripple adder, as well as some of the other adders, a pure carry-look ahead adder has high logic costs. Furthermore, high fan-in and fan-out requirements can be problematic: the fan-out required of the  $G_i$  and  $P_i$  signals grows rapidly with  $n$ , as does the fan-in required to form  $C_i$ . For sufficiently large values of  $n$ , the high fan-in and fan-out requirements will result in low performance, high cost, or designs that simply cannot be realized.

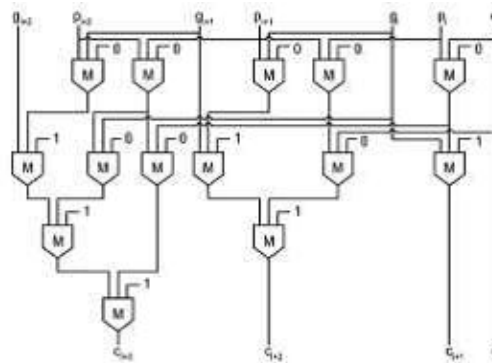


Fig 8: Carry block

This carry block is cascaded with the propagate and generate block. So, that carry is obtained with the following equation.

$C_i = G_i + P_i C_{i-1}$

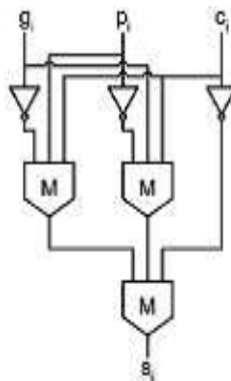


Fig 9: Sum block

This sum block is cascaded with the above carry block to obtain the sum. The following equation gives the sum bit  $S_i = P_i \oplus C_{i-1}$ .

The following shows the carry block which generate the carry bits.

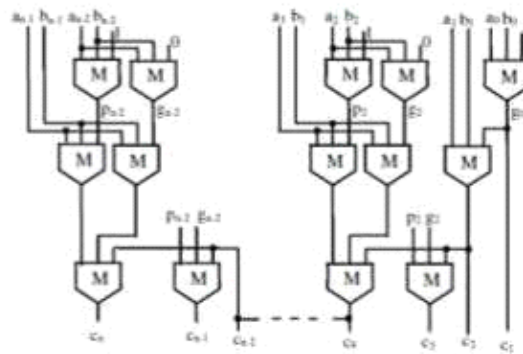


Fig 11: Carry block

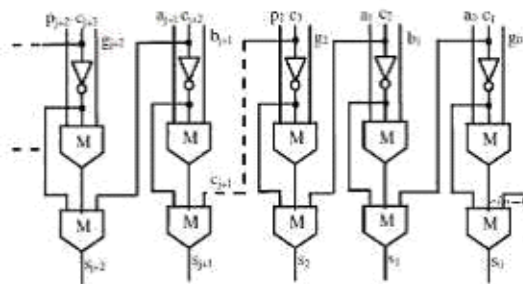


Fig 12: Sum block

The above carry block is cascaded with the sum block which generate the sum bits. The following are the equations for the carry bits and the sum bits.

$$C_{i+2} = M(M(a_{i+1}, b_{i+1}, G_i)M(a_{i+1}, b_{i+1}, P_i)C_i)$$

For sum block:

For odd

$$S_{j+1} = M(\sim C_j + 3M(a_{j+2}, \sim C_{j+3}, b_{j+2}), C_{j+2})$$

For even

$$S_{j+2} = M(\sim C_j + 3M(P_{j+2}, \sim C_{j+3}, G_{j+2}), C_{j+2})$$

### V. IMPLEMENTATION AND RESULTS:

The implementation of the proposed system using Verilog Hardware Description Languages and the simulation Results are as follows

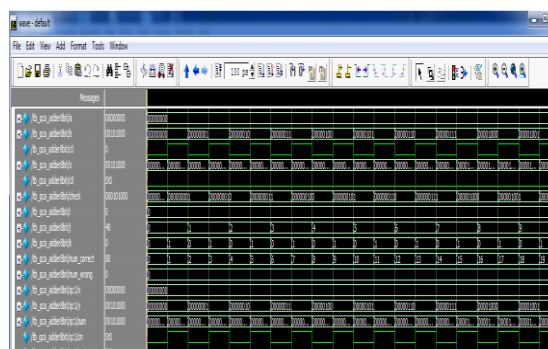


Fig simulation result of encryption

### VI. CONCLUSION

A new adder designed in QCA was presented. It achieved speed performances higher than all the existing QCA adders, with an area requirement comparable with the cheap RCA and CFA demonstrated in [13] and [16]. The novel adder operated in the RCA fashion, but it could propagate a carry signal through a number of cascaded MGs significantly lower than conventional RCA adders. In addition, because of the adopted basic logic and layout strategy, the number of clock cycles required for completing the elaboration was limited. A

128-bit binary adder designed as described in this brief exhibited a delay of only seventeen clock cycles, occupied an active area of 32.25  $\mu\text{m}^2$ , and achieved an ADP of only 548.25.

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